DELIVERING ON THE PROMISE OF CHIPS AND SCIENCE

Catalyzing Semiconductor Innovation through a National Semiconductor Technology Center

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Harvard John A. Paulson
School of Engineering
and Applied Sciences

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AUTHORS

Nathan Drucker (Harvard John A. Paulson School of Engineering and Applied Sciences)

Anushka Shah (The Fletcher School, Tufts University)

Ariel Higuchi, *CHIPS and Science Series Project Lead* (Harvard Kennedy School)

Amritha Jayanti (Harvard Kennedy School)

REVIEWERS

Edlyn V. Levine (America's Frontier Fund)

Venkatesh Narayanamurti (Harvard University)

Chris Miller (The Fletcher School, Tufts University)

Gregg Bartlett (GlobalFoundries)

Bill Bonvillian (MIT)

The authors would also like to thank countless others who provided helpful insight and feedback.

FACULTY PRIMARY INVESTIGATOR

Francis J. Doyle III, Dean, Harvard John A. Paulson School of Engineering and Applied Sciences

Venkatesh Narayanamurti, Benjamin Peirce Professor of Technology and Public Policy, Engineering and Applied Sciences, and Physics, Emeritus, Harvard University

This paper series was designed to provide a brief overview of specific issues identified in the Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act of 2022. These papers are not meant to be exhaustive.

Technology and Public Purpose Project
Belfer Center for Science and International Affairs
Harvard Kennedy School
79 John F. Kennedy Street, Cambridge, MA 02138

www.belfercenter.org/TAPP

Harvard John A. Paulson School of Engineering and Applied Sciences
29 Oxford Street, Cambridge, MA 02138

www.seas.harvard.edu

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Delivering on the Promise of CHIPS and Science Report Series

This report is part of a four-part series of research primers produced by the Technology and Public Purpose (TAPP) Project focused on the implementation of the 2022 CHIPS and Science Act.

Report Topics

1. Lab-to-Market Translation at NSF's Technology, Innovation, and Partnerships (TIP) Directorate
2. Community Colleges and the Semiconductor Workforce
3. Standard Setting: Process, Politics, and the CHIPS Program
4. Catalyzing Semiconductor Innovation through a National Semiconductor Technology Center

Each report topic formed the basis of a discussion organized by the Boston Tech Hub Faculty Working Group.

About the Boston Tech Hub Faculty Working Group

The Boston Tech Hub Faculty Working Group (FWG) was founded by former Secretary of Defense and Belfer Center Director Ash Carter and Harvard John A. Paulson School of Engineering and Applied Sciences Dean Frank Doyle. From February to May 2023, the group held monthly discussion-based meetings with senior faculty across Harvard and MIT and practitioners/decision makers across the public and private sectors that sought to explore and answer the questions: "How do we execute on the promise of the CHIPS and Science Act in an effective way?" and "Where do we go from here?"

The report authors would like to thank the Boston Tech Hub Faculty Working Group speakers and attendees for their contributions to each session.

Session Topics

- "Advancing Strategic Translational Science at the newly authorized TIP Directorate."
  Guest Speakers: Erwin Gianchandani, Stacey Dixon, Edlyn Levine, Steven Currall
- "Leveraging America's Potential - Workforce Development for the Semiconductor Industry."
  Guest Speakers: Sujai Shivakumar, Bo Machayo, Anastasia Urtz, Jared Ashcroft, John Katko
- "Standard Setting and CHIPS Legislation Implementation."
  Guest Speakers: Naomi Wilson, Mary Saunders, Andrew Updegrove
- "Catalyzing Semiconductor Innovation through a National Semiconductor Technology Center."
  Guest Speakers: Susie Armstrong, Jim Cable, Dev Shenoy, Gregg Bartlett

Executive Summary

The National Semiconductor Technology Center (NSTC) is intended to be the central hub for research and engineering within the semiconductor ecosystem.[1] It operates under the Department of Commerce and has the mandate to "advance and enable disruptive innovation to provide U.S. leadership in the industries of the future." The NSTC along with the National Advanced Packaging Manufacturing Program (NAPMP) has received $11 billion of the total $52 billion allocated in the CHIPS legislation. Recently, the Department of Commerce released a vision and strategy paper outlining three main goals for the NSTC:

- "Extend U.S. leadership in foundational technologies for future applications and industries and strengthen the U.S. semiconductor manufacturing ecosystem."
- "Reduce significantly the time and cost to prototype innovative ideas for member organizations."
- "Build and sustain a semiconductor workforce development ecosystem."

To achieve these objectives, the NSTC will prioritize "lab-to-fab" research, with a focus on a 5 to 15 year time frame. The shared facilities within the NSTC will prioritize flexibility over profitability. Unlike similar centers focused on national security for the Department of Defense (such as the Microelectronics Commons), the NSTC will concentrate on technologies for commercial development and involve various government agencies beyond the Department of Commerce.

The NSTC must develop new and innovative strategies for organizing semiconductor research and development (R&D). The $11 billion allocated to R&D by the CHIPS Act is a drop in the bucket of what many consider to be a required investment for meaningful semiconductor innovation. In this primer, we discuss key implementation strategies for the NSTC to achieve its first two goals (a separate primer on workforce development has been published, see below).[2] **We take note of strategic elements which have been raised by the NSTC vision paper, but also find opportunities to delve into the socioeconomic and geopolitical context of the CHIPS legislation, the infrastructure supporting the NSTC, and crucial business considerations for its success. Specifically, we highlight the potential benefits for smaller and medium-sized enterprises, which stand to gain the most from the NSTC.**

Organization of the Primer

This primer focuses on the R&D infrastructure authorized by the CHIPS and Science Act, specifically the NSTC. Our main objective is to address the central question: ***How can the NSTC and the associated semiconductor R&D network catalyze paradigm-shifting innovation and leverage the initial $11 Billion investment for greater returns over several decades?***[3]

- **Part 1** provides an overview of the geopolitical and economic context that led to the passage of the CHIPS+ legislation. We emphasize the role of offshoring manufacturing production to Eastern Asia and the strategic chokepoints it has created. **A major contributing factor to these chokepoints is the dominance of centralized monopolies in key elements of the manufacturing process**, such as Taiwan Semiconductor Manufacturing Company (TSMC) and Samsung in cutting-edge chip production, and ASML with the required tools.
    - We will also discuss several key challenges faced by smaller players in the semiconductor innovation ecosystem. These challenges include the **"valley of death,"** the lack of **scale-up funding**, and the importance of **de-risking investments** through competitive guaranteed contracts.
- **Part 2** focuses on the infrastructure challenges faced by semiconductor innovation, especially from the perspective of smaller- and medium-sized companies (SMEs). We explore the role of different-sized foundries, such as coupon, 200mm, and 300mm, and how the NSTC can leverage existing facilities to distribute the demand for prototyping and scaling up.
- **Part 3** delves into the business structures of government-backed projects, including the role of intellectual property and funding in user facilities. The significant investment made by the industry in R&D results in valuable intellectual property, including patents, trade secrets, source code, and more. SMEs face challenges regarding the protection of their intellectual property and maintaining independence within consortia that consist of much larger companies. Consequently, safeguarding this intellectual property becomes crucial for the industry to maintain its competitive position globally. This section also explores different business models employed in rapid lab-to-fab innovation, such as the NASA Commercial Orbital Transportation Services (COTS) program and Operation Warp Speed. The central objective of these business models is to mitigate risk by providing government-backed loans and guaranteeing customers, whether they are other private entities or the government itself.

Key Concepts

- **"Valley of Death"** refers to the gap in available resources between early-stage R&D typically done at Universities and National Labs, and that available through private investors specifically for taking demonstrated products to market. This term is especially applicable to innovation in the semiconductor manufacturing sector, among other deep/hard tech sectors where early capital costs beyond lab demonstration are prohibitive.
- **"Scale-up Funding"** is required even after prototypes have been demonstrated and early venture capital money has been acquired. Building out a fabrication process is typically the most capital-intensive stage of the semiconductor manufacturing innovation cycle, as it requires its own forms of optimization for the standard high volumes of devices seen across the industry. There is another large gap in funding at this stage of the innovation process.
- **"De-risking"** new technologies is an essential part of the innovation process. Many large corporations such as TSMC and Samsung do not risk investing in potentially paradigm-shifting R&D because the opportunity cost is too high to interrupt their high-yield processes. For smaller companies, cutting-edge R&D may face a challenging entry into the market. The government can play a central role in mitigating these effects by establishing demand.

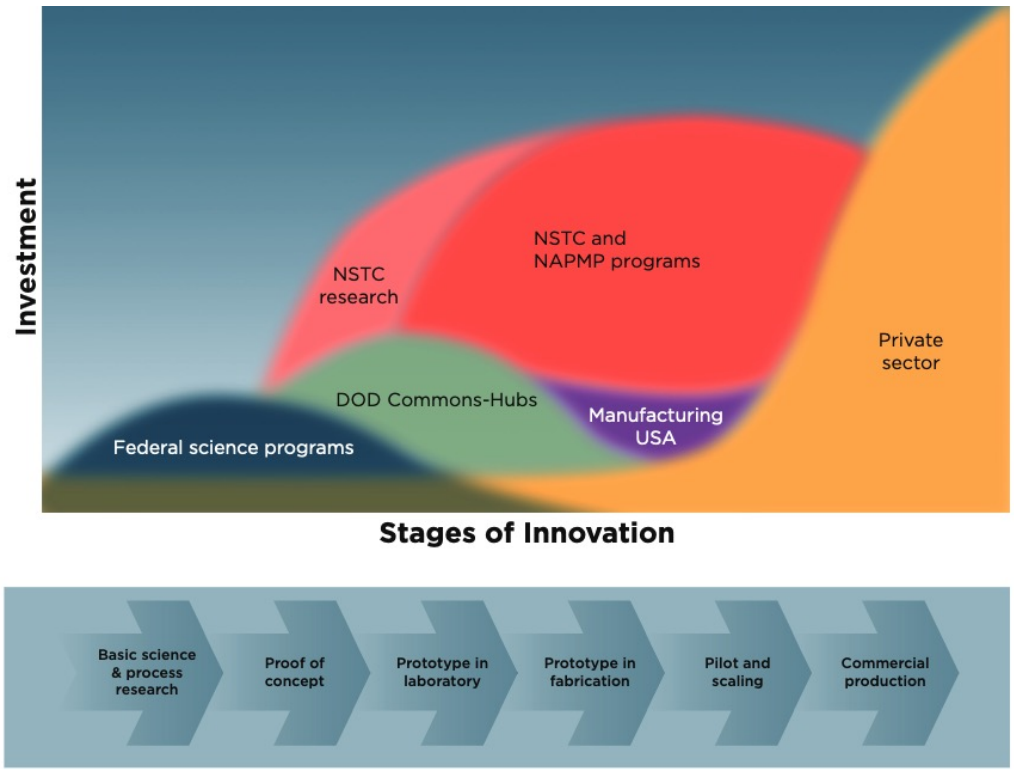

Figure 1. Reprinted from A Vision and Strategy for the National Semiconductor Technology Center[4]

Introduction

On April 25, 2023, the CHIPS for America Research and Development Office unveiled *A Vision and Strategy for the National Semiconductor Technology Center* report.[5] This document outlines the goals and objectives of the NSTC, which play a crucial role in the CHIPS Act's investment in securing America's position as a global leader in semiconductor technology and innovation. The CHIPS Act consists of two funding categories: $39 billion in incentives for U.S.-based manufacturing facilities and $11 billion in R&D funding to ensure ongoing U.S. leadership in emerging semiconductor technology.[6]

The NSTC is an integral part of a comprehensive government strategy aimed at advancing and enabling innovations in microelectronics R&D. It has three main high-level objectives. First, it aims to extend America's leadership in semiconductor technology. Second, it seeks to reduce the time and cost involved in transitioning from design concepts to commercialization. Last, it aims to build and maintain an ecosystem for semiconductor workforce development.[7]

The NSTC will bring together a wide range of stakeholders, including government agencies, national laboratories, industry, workforce representatives, customers, suppliers, educational institutions, entrepreneurs, and investors. Members will have access to research, facilities, workforce programs, convenings, shared roadmaps, standards development, and data sets. The NSTC will focus on three key program areas: technology leadership, managing assets for community benefit, and workforce programs. It will foster an open and collaborative research environment while ensuring the protection of proprietary information. The NSTC will work closely with the National Advanced Packaging Manufacturing Program to provide resources for NSTC members, including advanced packaging facilities and chiplet programs.

The implementation of the NSTC is a significant step toward promoting technological innovation in the country. It has the potential to drive innovation and economic growth, attract foreign investment, and create more job opportunities for citizens. However, it is important to acknowledge that the success of this policy relies on the government's ability to provide adequate support to startups and small- and medium-sized enterprises. These businesses form the backbone of any thriving innovation ecosystem and require significant support to grow and scale. Therefore, it is imperative for the government to grant them access to funding, infrastructure, and other resources to help them thrive and contribute to the growth of the economy.

Part 1: Socioeconomic and Geopolitical Context

What geopolitical factors led to the creation and passage of the CHIPS and Science Act?

- **Demand for semiconductors is increasing for civil, consumer, and military applications.** The progress of modern society, driven by digitization and technological advancements, heavily relies on developments in semiconductor-based technologies. Demand for sensing, computing and memory is on the rise over the long-term.[8] These capabilities are integrated into vital infrastructure and military capabilities, making it imperative to lead technological advancement and shore up existing gaps within domestic production capabilities.

- **Advanced semiconductor manufacturing is a national security issue.** Maintaining technological superiority is a key strategy of the U.S. military. Advanced sensing and computation capabilities are actively being developed and integrated into military systems. The development of semiconductor technology heralds back to the drive for asymmetric capabilities during the Cold War.[9] From this perspective, the bipartisan support for the CHIPS and Science Act was driven by national security concerns surrounding semiconductor manufacturing.

- **The global share of American domestic semiconductor manufacturing capacity has declined from 37 percent in 1990 to 12 percent at present.**[10] While the initial development of the semiconductor industry occurred in the United States through companies like Intel (successor of Fairchild Semiconductor) and Texas Instruments, American companies no longer lead in the most advanced manufacturing processes.[11] The advent of chip design software advancements in the 1980s and the foundry model pioneered by TSMC made it easier for American companies to design chips domestically and outsource production overseas. This shift was accompanied by changes in corporate governance which prioritized low manufacturing costs abroad over maintaining domestic capacity.[12] While American companies still excel in chip design, only two companies, TSMC in Taiwan and Samsung in South Korea, dominate leading-edge logic chip production.

- **China has made substantial efforts to enhance its semiconductor manufacturing capabilities with the aim of becoming the global leader by 2049.**[13] In certain aspects, China's semiconductor manufacturing base is in an even more precarious position than that of the United States. The United States and its strategic allies exert significant control over almost every aspect of the global semiconductor supply chain, giving them the ability to manipulate it and limit China's access to critical semiconductors. Semiconductor manufacturing has been identified as a crucial industrial policy in China's Five-year Plans, and the country intends to establish dominance in this sector

within the next few decades. China has made substantial investments, specifically allocating an estimated $150 billion to the semiconductor industry over the past five years.[14]

- **The COVID-19 pandemic highlighted the vulnerabilities in global supply chains, with the semiconductor industry being no exception.**[15] The acute shortage of chips during the pandemic significantly impacted the automotive industry, and consumers experienced price increases in products such as graphics processing units (GPUs), partly due to a major fire at a Taiwanese factory.[16] The need to reorganize and secure supply chains extends beyond semiconductors, but the pressure is particularly pressing in the semiconductor ecosystem due to the limited redundancy of manufacturing capabilities.

- **Taiwan and South Korea, home to the most advanced logic chip manufacturing, are situated in geopolitical hotspots, contributing to increased tensions.** Samsung and TSMC are leading manufacturers of logic chips, but both operate in geopolitical "hot zones" affected by rising tensions between China and the U.S.[17] Taiwan, in particular, is facing ongoing pressure due to the Chinese Communist Party's desire for reunification. Toward this end, the global economy would suffer greatly if Taiwanese fabs became inaccessible due to potential Chinese aggression.[18]

- **While advanced logic manufacturing is necessary for cutting-edge devices, the majority of the market demand actually lies for more mature devices.** Companies like Apple, Qualcomm, and NVIDIA Corporation are major customers for the most precise foundries such as TSMC and Samsung. However, commercial applications of mature-node semiconductor devices in sectors such as aerospace and automotive also drive the industry and do not necessarily require cutting-edge chips. Despite the intense focus on bleeding-edge processes, older legacy nodes—which serve numerous applications—receive less attention but present significant opportunities for innovation.[19]

2022 Total Global Semiconductor Market: $574 Billion

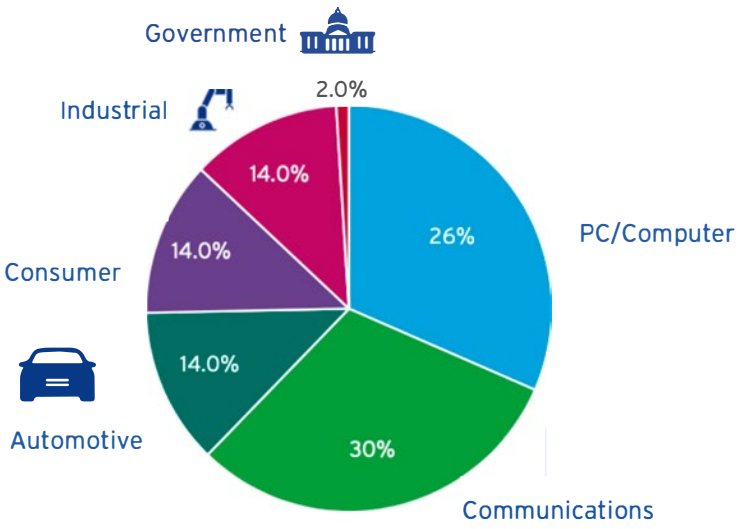

Figure 2. Reprinted from Semiconductor Industry Association's "2023 Factbook."[20]

Key Insights and the Role of the NSTC

- **The concentration of manufacturing power in the hands of very few companies and countries creates risks within the semiconductor supply chain and innovation process.** The major chokepoints in the semiconductor industry arise because a handful of companies in only a few countries have the necessary capital intensity and unique manufacturing capabilities for the most advanced fabrication. In some respects, these nodes are "too big to fail" and heavily influence policy and innovation. While large companies like TSMC invest heavily in optimizing leading-edge processes, they do not have as much incentive to invest in paradigm-shifting, "beyond-the-road-map" new technologies.[21]

- **Currently, there is a tremendous opportunity for the emergence of breakthrough computing paradigms.** Moore's Law, which states that the number of transistors per unit area in a chip should double every two years, is coming to an end as transistors reach fundamental physics barriers and packing them closer together becomes too expensive.[22] Technologies that go beyond the traditional roadmap for decreasing transistor size, such as quantum computing and AI-specific integrated circuits, have garnered a lot of attention. Stakeholders from across academia, government, and industry are developing next-generation computing systems. While larger firms are continuing to pursue smaller transistor sizes along with Moore's law, it is often smaller, more nimble entities that seek to develop paradigm-shifting, breakthrough computing technologies.

- **Smaller companies often have innovative technologies but face difficulties gaining a foothold in the semiconductor industry.** Entrepreneurship is a primary mechanism for innovation in any industry.[23] However, the extremely high capital costs required for manufacturing semiconductors make it challenging for small companies with limited capital to establish themselves in this sector. Moreover, how small companies can acquire capital, primarily through venture capital, systemically disfavors hard/deep tech that bridges the gap from proof-of-concept to initial production (called the "Valley of Death") and from initial production to large scale manufacturing (scale-up funding). This problem is exacerbated in the semiconductor industry when time to market can be long, and capital costs are extremely high. This perilous innovation landscape makes investing in new, potentially revolutionary technology very risky.

- **A key mission for the NSTC is making the process of semiconductor innovation easier.** Secretary Gina Raimondo has asserted that if properly executed, "by the end of the decade, we'll cut in half the projected cost of moving a new chip from concept to commercialization."[24] This process can be twofold. On the one hand, the NSTC and its associated network can strategically assist SMEs which are key drivers of innovation. On the other hand, the NSTC must establish a revolutionary innovation infrastructure that integrates facilities across a well-coordinated ecosystem focusing on solving critical innovation challenges within the semiconductor industry, such as lowering the costs of innovation itself.

Part 2: Designing the NSTC

What kinds of infrastructure are involved in semiconductor manufacturing?

- **Semiconductor manufacturing is arguably the most advanced form of manufacturing, requiring some of the most sophisticated and precise tools ever created by humankind.** The constant increase in computing power over the past 70 years can be attributed to the miniaturization of transistors—electronic switches—by nine orders of magnitude. Early computers were powered by large and faulty vacuum tubes. The transistor, which was invented in 1947 at Bell Labs, was the size of an eraser head. Today, the smallest transistors are only 20nm wide (despite the title 'single-digit nanometer nodes'). This miniaturization has led to approximately doubling computing power every two years, known as Moore's Law.[25]
    - To make these devices so small requires tools with atomic scale precision which cost billions of dollars to develop and hundreds of millions to purchase.[26] Only a handful of companies in the world have the resources to develop and utilize these cutting-edge tools.
    - In addition to the high cost of fundamental tools, the facilities necessary for manufacturing are also costly. The nanofabrication process must take place in a cleanroom, which is a highly controlled environment designed to prevent dust and other particulate matter from compromising device performance.
- **Developing new devices takes years, and even longer to optimize them on a production line specialized in creating features of a specific size (node).** There are three primary categories of devices made in the semiconductor sector: **memory** for storing information; **logic,** for manipulating (computing) information; and **discrete, analog, and other devices** for gathering information. Among these, advanced logic devices currently require the smallest feature sizes on the order of nanometers while many other devices can be made with legacy tools.
    - Devices are produced in high-yield processes with several key steps:
        1. **Deposition.** Atomically thin layers of metals, semiconductors, and insulators are grown on top of silicon wafer substrates. These sheets are eventually 'cut' by the next steps to form devices.
        2. **Lithography.** Light sensitive chemicals–photoresists– are coated onto the wafers so that computer designed patterns can be defined by exposing the wafer to light. Making small devices requires ultraviolet (UV) light, which has a wavelength of a similar size to the desired device size (tens to hundreds of nanometers).

3. **Etching.** This is the process by which materials exposed through lithography are removed, either through wet chemical reactions or with gases. As a result of the etch step, device architectures are defined.

4. **Packaging.** With the silicon wafer full of identical devices, each one must be individually cut out and integrated into a larger circuit. These circuits contain many other components and ultimately are the devices users interface with.

Each of these steps requires very sophisticated machinery. Usually, the equipment can only handle silicon wafers of a given diameter. The highest yield, most expensive tools operate on 300mm diameter silicon wafers, whereas older (or legacy/mature) tools operate on 200mm (and smaller) wafers. In addition to operating on wafers of different diameters, tools have varying degrees of precision (up to tens of nanometers on cutting-edge tools).

- **The CHIPS and Science Act has established a total of five institutions to address issues in the semiconductor manufacturing process**. These include the NSTC, National Advanced Packaging Manufacturing Program (NAPMP), and three new Advanced Manufacturing Institutes. These centers are intended to focus on technologies at different stages of the innovation cycle. In its vision paper for the NSTC, the Department of Commerce states that the NSTC should focus on technologies that will be ready for market in 5 to 15 years.[27] Meanwhile, the NAPMP will potentially focus on integrating different kinds of devices with new forms of advanced packaging.
- **Due to the high cost associated with developing new devices, smaller companies and university researchers struggle to access the resources they need for innovation. A central role for the NSTC should be reducing capital costs for smaller companies by providing critical access to lab space and services.** Across the deep/hard tech sectors, new models of institutions have emerged which aim to leverage shared lab space to reduce costs for participating companies. For example, within the semiconductor sector, constructing cleanroom facilities is prohibitively expensive for individual smaller companies, but they may be interested in purchasing an exclusive tool to use in such a space.
- **The NSTC should coordinate across the network of existing facilities and consortia.** Several nanofabrication facilities provided by different government organizations, such as the Department of Defense (DoD), NSF, NIST, and Department of Energy, offer access for non-proprietary and proprietary research. Coordination across these facilities will ensure greater efficiency in the long run and help the NSTC address specific technical areas while its facilities are under construction. In addition to federal research facilities, there are university labs, public-private partnership labs like NY Creates, and purely private sector government contractors with whom the NSTC should coordinate. With a strong coordination structure, the NSTC will not need to own the entire toolset and can create voucher programs or other subsidies to incentivize other organizations to participate.[28]

- **The NSTC can learn from the organizational structures of several institutions that serve lower-throughput, proof-of-concept devices.** Institutions like imec in Belgium and MIT Lincoln Labs play a critical role in manufacturing devices that require validation and optimization, even starting with nanofabrication facilities at universities. Since 300mm wafer-scale processes are expensive, there is not much experimentation that can be done on these foundry lines. As a result, smaller 200mm tools provide the flexibility needed in this kind of environment. Even smaller lines that use coupon-sized (test) processes would be useful for earlier stage devices. Facilities like imec also have tools for 300mm processing available once devices have been demonstrated on other lines. Nevertheless, since the tools are so expensive to use, startups are often a lower priority at these facilities compared to established large companies.
- **In addition to providing space for smaller companies to develop their ideas, the NSTC should allocate significant resources to developing better methods for semiconductor innovation itself**. Even in a seemingly simple process such as changing the wafer size used in a fabrication line, there are tremendous technical difficulties. Translating devices from coupon chip sizes to 200mm and eventually 300mm wafers is extremely challenging and warrants exploration on its own. Across the whole spectrum of device design and fabrication, there are opportunities to reduce capital costs, as was done with the revolution in device design. By figuring out how to innovate more efficiently, the NSTC can enable entirely new industries and accelerate technical development.
- **Investment into tool development and materials processing can have a tremendous impact across the innovation spectrum.** Innovation in advanced tools and materials enables other technologies. For example, the investments made across the industry into extreme UV (EUV) lithography tools enabled the smallest semiconductor devices we have today. Similarly, emerging applications in next-generation wireless networks and power electronics require materials other than silicon—namely silicon-carbide (SiC) and gallium-nitride (GaN)—for optimal efficiency. Integrating these materials into current processes is costly but potentially high reward. In addition, investment into material and tool processes can spill over into other interdisciplinary fields, such as the interface between nanotechnology and biotechnology with potentially substantial impact.

How do other institutions organize their infrastructure to achieve diverse and effective user spaces?

- **imec:** Based in Leuven, Belgium, imec is a primary chips R&D hub in Europe. It was founded in the 1980s as an inter-university consortium with help from the Flemish government. Its partnership with companies for R&D has led to its revenue growing from tens of millions of Euros at its founding to over €700 million today.[29]
    - **Infrastructure**: imec has two primary facilities: a 300 mm cleanroom with leading-edge capabilities and a 200mm cleanroom with more flexible processes for prototyping devices that

foundries would not normally support. By having both capabilities, imec can cater to companies from across the full stack of semiconductor manufacturing. Those with a need for higher volume can use the 300mm processes, while stakeholders who may be trying entirely new devices like ASICS (application-specific integrated circuits) can use the 200mm cleanroom.

  - **Business:** The Belgian government is the largest stakeholder at imec, providing 16 percent of the funding. The largest member companies each provide no more than 4 percent of the total funding which in some ways maintains the facility's neutrality.[30] While the facility plays a key role for larger companies like TSMC, it also offers programs aimed at smaller enterprises. These include access to imec's infrastructure and internet protocol (IP) directly, designated teams of strategists to advise startups and a venture fund for direct investment. As a centralized facility, imec achieves the revenue necessary for sustainability through partnerships with large companies while also providing programs and facilities to help smaller companies grow.

- **MIT Lincoln labs:** MIT Lincoln Labs is a federally funded R&D center (FFRDC) chartered by the DoD and operated by MIT. Its primary goal is to develop advanced technology for national security applications. Lincoln Labs maintains a variety of facilities to this end, including a nanofabrication facility for device prototyping and scaling. Among all U.S. government semiconductor fabrication facilities across different agencies, Lincoln Labs is considered to be the most effective.[31]

  - **Infrastructure:** The primary fabrication facility at Lincoln Labs uses 200mm tools. Although these tools do not produce at the same scale as 300mm tools in facilities at companies like TSMC, they provide the flexibility Lincoln Labs needs to develop and scale new devices. These tools are not only used for cutting-edge complementary metal-oxide semiconductor or CMOS technologies, but also for next-generation devices. For example, Lincoln Labs facilities can fabricate some of the best superconducting devices for quantum information technologies.

  - **Business:** As a FFRDC, Lincoln Labs does not sell its devices. Nevertheless, the facility plays a key role in demonstration and early scale-up of new devices. For instance, there is a tight collaboration between MIT's academic research community and the fabrication facilities at Lincoln Labs, which enables the translation of critical technologies. Another crucial aspect of Lincoln Lab's success is its certification as a DoD Trusted Foundry. This accreditation, as well as its status as a DoD facility, establishes the steady demand for Lincoln Labs' technologies and plays a role in de-risking the technologies it produces.

Part 3: Business Models for the NSTC

Intellectual Property Regulations, Partnership Models, and Financial Instruments

- **The substantial investment made by the semiconductor industry in R&D results in valuable intellectual property such as patents, trade secrets, source code, and more.**[32] For SMEs, IP is key to generating value before large customer bases have been established. SMEs and startups have concerns about protecting IP and maintaining independence within consortia containing much larger companies. Therefore, safeguarding this intellectual property is crucial for the industry to maintain its competitive position globally.

- **Sharing intellectual property is critical for reducing barriers to semiconductor innovation.** One major hurdle for small- and medium-sized enterprises in the semiconductor sector is the high cost of accessing necessary licenses for new device development. However, there are significant opportunities for innovation when ideas can be built at low cost. For instance, integrating different types of devices can enhance overall performance, but it requires access to expensive intellectual property. In some cases, a company may require assistance in developing a fabrication process that others have already developed but are hesitant to share, resulting in increased time and cost investments. The Department of Commerce's vision paper for the NSTC recognizes the importance of IP sharing within the facility and across its network.[33]

- **NSTC should establish a framework that facilitates IP agreements among its collaborators to prevent private entities from experiencing IP loss when providing access to state-of-the-art facilities or making foundational contributions.** Such a framework should be considered a prerequisite for participation in the NSTC network. To foster a relationship between SMEs and large entities, incentives should be provided to both parties. Various solutions can be explored, such as implementing a royalty model that allows accessible pricing structures for SMEs or users to access NSTC facilities owned and/or operated by large private entities. This approach would incentivize facility providers to increase access and support the success of users. NSTC should also establish a framework that facilitates IP agreements among its collaborators, taking into account previous experiences with semi-SEMATECH, SEMATECH, and the Semiconductor Research Corporation. Understanding what worked or did not work in those initiatives is crucial, as the semiconductor industry's IP landscape differs significantly from that of the biotech and software industries. Cross-licensing is one of the key mechanisms employed in the semiconductor industry, playing a major role in fostering collaboration and innovation.

- **Challenges arising from IP risks are likely to impact collaborations at all stages within the NSTC, including early-stage research, design and proof-of-concept collaborations, and**

middle- and late-stage prototyping collaborations. However, early-stage research collaborations face unique challenges related to cost, time, and expertise. Large entities with abundant resources and expertise may dominate the patenting process of early-stage research and secure rights to immature technologies. This often results in smaller entities, including small- and medium-sized businesses, facing significant burdens in terms of cost and resource allocation to file patents prior to discovery, especially given the "first to file" patent law.

- **The U.S. government is entitled to unlimited IP licensing rights from projects that it funds, as established by the Bayh-Dole Act.**[34] To prevent disincentivizing entities from participating in the NSTC, the Department of Commerce may consider several approaches. For example, advanced purchase of fab capacity as a service for the government could be explored instead of directly funding an infrastructure project. This model could have limited IP implications and has been successfully utilized by other programs to enable competition and alleviate cost burdens while receiving necessary launch services. Another approach involves aggregating and pooling purchasing demand for various semiconductor services, such as fab, manufacturing, and advanced packaging, across the ecosystem, including large automotive and consumer electronics companies. This approach can help drive initial infrastructure investment directly from the private sector rather than the government. Alternatively, leveraging a trusted non-profit investment broker to receive federal funding and disperse it to eligible entities could protect recipients from IP loss and allow for simplified equitable access for SMEs, while fostering collaboration across the entire ecosystem. The trusted broker must adopt a whole-of-government and whole-of-sector approach to ensure effectiveness.

- **The NSTC could also identify areas within legislation where incentives can be broadened, or impediments can be eliminated to encourage companies to engage in innovation.** This could involve reinforcing and clarifying the authorities of the national security innovation base to permit more adaptable approaches, such as more accommodating procurement and funding processes that facilitate the conversion of R&D efforts into deployable technology.

- **NSTC can learn from several examples of successful and unsuccessful business models for public-private partnership programs in the semiconductor industry and beyond.** Insights can be gained from a range of public-private partnership programs in the semiconductor industry and beyond, including NASA's successful COTS program for commercial cargo transportation, Operation Warpspeed's rapid COVID-19 vaccine development initiative, and the SEMATECH semiconductor consortium. Although the SEMATECH consortium did not achieve the desired outcomes, it played a significant role in developing EUV lithography and transitioning to 300mm tool sets.[35] These examples illustrate critical factors that can determine the success or failure of such collaborations for driving innovation.

NASA COTS

Background: The NASA Commercial Orbital Transportation Services (COTS program was established in 2006 with the aim of developing commercial cargo transportation services to the International Space Station and reducing NASA's reliance on Russian launch vehicles.

- **Market dynamics:** The COTS program was launched in response to the need to reduce NASA's dependence on Russian launch vehicles, but also to encourage the development of a commercial space industry in the United States. The commercial space industry was emerging as a viable market, and NASA wanted to capitalize on this trend by partnering with commercial entities to provide cargo transport to the ISS.
- **Funding:** The COTS program operated as a public-private partnership, with NASA contributing seed money for development while commercial partners covered over 50 percent of the development costs. Fixed price milestone payments incentivized cost control and minimized schedule delays. NASA's commitment to purchase operational services played a crucial role in enhancing the ability to secure funding. Although equipment transfer was initially considered in the Space Act Agreement (SAA), NASA lacked the statutory authority to provide Government Furnished Equipment under the COTS program. Consequently, the program had to rely on loan agreements and cumbersome General Services Administration procedures to facilitate the transfer of equipment required for berthing with the ISS. Nonetheless, additional funding was allocated later in the program to conduct further risk reduction testing, which directly contributed to the successful first attempt berthing of SpaceX Dragon to the ISS.
- **Program focus:** The primary focus of the COTS program was to develop cargo transportation services specifically for the International Space Station, which was critical for NASA's operations. While the program aimed to foster innovation and reduce life cycle development costs, it did not address broader industry issues such as human spaceflight, deep space exploration, or the market demand for commercial space services. Consequently, the program's impact on the overall space industry remained limited.
- **Interface requirements:** Establishing minimum firm requirements and ensuring appropriate government oversight were crucial in promoting innovation and minimizing life cycle development costs. Goals (vs. requirements) were established to allow for flexibility in trade space and design optimization. Firm requirements were only specified when necessary to ensure the safety of the ISS and its crew. The ISS interface requirements for COTS evolved over time, with active involvement and collaboration between NASA and its commercial partners. A diverse portfolio of partners with varying capabilities ensured a balanced approach to technical and business risks. Encouraging commercial-friendly intellectual property/data rights and limiting termination liability played a vital role in attracting private capital investment.

OPERATION WARP SPEED (OWS)

- The goal of OWS was to develop a vaccine against the COVID-19 pandemic as quickly as possible. Initially, it received $10 billion in funding authorized by the Coronavirus Air, Relief and Economic Security (CARES) Act, which is a significant amount comparable to the funding allocated for the NSTC. Importantly, OWS operated as an independent task force that drew participants from various organizations including the Centers for Disease Control, National Institutes of Health, Department of Defense, and the Food and Drug Administration. By leveraging staff and resources from multiple agencies while maintaining an independent status, the program maximized the utilization of federal resources without being hindered by typical interagency processes.[36] In addition to federal participants, OWS implemented a competitive selection process for private sector participants. Initially, eight companies were awarded seed money, each with a different technical approach to vaccine development. However, only a few of these companies successfully completed the expedited FDA approval process.

  Another crucial aspect of the program was the guarantee provided by the U.S. government and other nations worldwide that a market would exist for the vaccines once they were developed. Similar to the NASA COTS program, the demand created by guaranteed buyers reduced the investment risk for companies and provided incentives for them to develop innovative solutions.

SEMATECH

- Established in 1987, SEMATECH was a public-private partnership created with the aim of revitalizing the U.S. semiconductor industry. Its primary objective was to regain advanced technological leadership after Japan's rapid rise in high-quality, low-cost semiconductor manufacturing. SEMATECH facilitated R&D efforts, fostered collaboration among semiconductor manufacturers, and promoted technology transfer. Initially, it achieved notable successes such as advancements in manufacturing techniques like EUV lithography. However, the organization faced challenges in the late 1990s, coinciding with the offshoring of domestic manufacturing capacity and the increasing popularity of fabless design.

  - **Market dynamics:** SEMATECH was established as a response to Japan's dominance in the memory chip market, with the United States falling behind. However, by the mid-1990s, Japan's economy was in decline, and Taiwan and South Korea had emerged as strong competitors. Additionally, the United States had shifted its focus to logic chips. As a result, the urgency to support the U.S. semiconductor industry diminished, making the need for SEMATECH less apparent.

- **Funding issues:** SEMATECH operated as a public-private partnership. However, as the industry grew more competitive, companies prioritized their individual R&D efforts over those of the partnership, resulting in a decline in private sector funding for SEMATECH. Moreover, the end of the DoD's five years of co-funding strained SEMATECH's budget, thereby making it challenging for the organization to sustain its R&D activities.

- **Narrow focus:** SEMATECH suffered from a poorly devised governance structure that failed to adapt to changing circumstances. While the consortium successfully emphasized manufacturing technology, including lithography and wafer fabrication, which played crucial roles in semiconductor production, it fell short in addressing broader industry issues. SEMATECH neglected concerns related to market structure, product innovation, and competition, which were essential for the industry's overall growth and competitiveness. For instance, it did not adequately address the emerging trends of offshoring manufacturing or the rise of the foundry model exemplified by TSMC. These significant industry shifts were not effectively incorporated into SEMATECH's agenda, limiting its impact and relevance in a rapidly evolving semiconductor landscape. The consortium's narrow focus on specific manufacturing technologies hindered its ability to address the broader challenges and dynamics reshaping the industry, ultimately limiting its long-term effectiveness.

Key Takeaways from NASA COTS, OWS, and SEMATECH for the NSTC

- **To mitigate risk, the NSTC should adopt a competitive, portfolio approach to its funding**. The concept of "picking winners" in industrial policy often receives criticism due to the potential for economically inefficient outcomes. For instance, the bankruptcy of solar cell manufacturer Solyndra, a major recipient of government loans, led to political backlash against the Department of Energy's advanced projects funding despite the successes of other ARPA-E programs.[37] By implementing competitive award processes and funding multiple stakeholders, the risk can be distributed. OWS serves as a successful example of the portfolio approach. OWS initially funded eight different companies but allowed market forces to determine the ultimate winners.[38] Another example—although to a lesser extent—is the NASA COTS program, which provided grants to several companies including SpaceX for the development of cost-effective space transportation systems.

- **The NSTC must play a role in de-risking technology through market creation and demand pull.** In the semiconductor innovation process, there is often a disconnect where new processes, devices, and materials may lack demand due to high implementation costs, thus hindering their development. By providing a guaranteed market on the demand side, companies are incentivized to pursue riskier projects with potentially higher rewards.

    - A good example of de-risking is the role of the DoD Trusted Foundry certification. Skywater and Global Foundries are some of the few foundries which are certified providers to the DoD,

and thus they benefit from the demand from the DoD. Similarly, Lincoln Labs is a certified facility and therefore its users have an easier path toward getting customers.

- Another example of de-risking is the NASA COTS program, which guaranteed NASA would purchase services from the final companies to launch into space.
- The companies funded by OWS also experienced this de-risking by having the government be a guaranteed buyer of resultant vaccines.
- Despite the role of the government as a procurer, it only makes up a small percentage of total market share. **Commercial partnerships between domestic semiconductor manufacturers and customers will be crucial for ensuring sustainable demand.** The NSTC and other bodies at the Department of Commerce can help establish these relationships.

- **The NSTC can collaborate with other government agencies to develop financing and transaction methods that create demand and reduce conventional burdens of government acquisition.** Conventional government contracts, while providing demand for advanced technologies, often favor larger companies and are accompanied by stringent requirements. The government can use other methods to more flexibly engage with other stakeholders, like SMEs.
  - **Advanced Market Commitments** provide a means to increase demand pull while leveraging efficiencies of the private sector.[39] These commitments have been prominently applied in the procurement of COVID-19 vaccines, where the U.S. government pledged to purchase successful vaccines upon their development. While the NSTC itself may not be directly responsible for such grants and loans, it can collaborate with other government agencies to coordinate their distribution. For instance, the Department of Commerce could facilitate agreements between semiconductor consumers (e.g., automotive companies) and semiconductor suppliers, commissioning foundries to produce a large number of devices for specific customers.
  - **Other Transactional Authorities (OTAs)** are employed by the DoD for research & development, prototyping, and production of technologies. Crucially, OTAs enable participation of non-traditional contractors like non-profits, academic institutions, and smaller companies by bypassing the typical requirements of the Federal Acquisition Regulation. Although the NSTC primarily focuses on developing technologies for commercial applications, some of these technologies may also have relevance for defense applications (dual-use). Future legislation could explore the establishment of OTAs for non-defense technologies.
  - The **Defense Production Act (DPA)** empowers the President to prioritize critical national defense needs, allocate resources, and exert control over the economy. Originally developed during the Cold War, the DPA continues to be frequently leveraged to address a range of issues, from nuclear submarine production to shortages of baby formula. Recently, President Biden signed a Presidential Determination authorizing the use of the DPA for printed circuit boards and advanced semiconductor packaging.[40]

- **The NSTC can help align goals across the semiconductor ecosystem.** Programs like OWS and NASA COTS had very specific technical goals: to create a vaccine for COVID-19 and develop orbital transportation capabilities, respectively. Arguably, having a clear goal, leads to success. One concise, clear goal may not be feasible in the broader semiconductor landscape, but having clear goals within specific programs at the NSTC will help with its efficacy. Although many goals of the semiconductor ecosystem are articulated by industry-wide roadmaps, there is tremendous opportunity for paradigm-shifting innovation beyond the roadmap.

The NSTC presents a unique opportunity to enhance America's semiconductor innovation system. Through the establishment of a shared facility that accommodates diverse stakeholders from different segments of the innovation cycle, the Department of Commerce can effectively reduce barriers to the adoption of paradigm-shifting technologies. However, the optimization of the NSTC, particularly to support SMEs, holds the greatest potential for advancing U.S. leadership in future advanced information technologies. Several critical strategies need to be employed to ensure the success of the NSTC, including bridging the "valley of death" and mitigating costs associated with potentially revolutionary semiconductor technologies. Vaccines were developed through Operation Warpspeed at an unprecedented speed with only $10 billion. How much the NSTC will be able to leverage out of a similar investment will not only be determined by the physical infrastructure of the facility but also by its governance and organizational culture.

It is worth noting that the design of the NSTC is still in its early stages. On June 6, 2023, the Department of Commerce announced the CHIPS for America R&D leaders.[41] The Department has indicated that additional information regarding the structure of the NSTC will be provided later this year.

Further Research to Guide NSTC Implementers

As the details of the NSTC, such as its specific location and infrastructure, are yet to materialize, there are several topics and questions beyond those addressed in this primer. The following are intended to be questions for further discussion and research among NSTC implementers and extend to other hard tech innovation catalysts.

- **Metrics of Success.** While the goals of the NSTC—to establish U.S. leadership and reduce the cost of innovation in the semiconductor industry—are clear, specific metrics of success should be defined by which the efficacy of the program can be evaluated during its lifetime. With diverse stakeholders from across the semiconductor ecosystem ranging from smaller academic and startup research teams to some of the world's largest multinational firms, it will be important to create a methodology by which consensus of the metrics will be reached.
- **Portfolio Management.** This primer has highlighted the role of the portfolio approach in mitigating stakeholder risk and has drawn attention to successful programs like Operation Warpspeed. Nevertheless, one drawback of the portfolio approach is that it risks distilling capital across the portfolio to an extent where critical funds are not achieved for anyone receiving funds.
    - This risk is particularly acute given the fact that the $11 billion investment in CHIPS R&D is considered by many experts to be a 'drop in the bucket' to solve the broader problems faced by the industry, and pales by comparison to investments made by other foreign governments. An inherent tension in the semiconductor ecosystem is that the capital intensity currently required to make a significant impact is so high that only a handful of firms can afford it.
    - In addition, many portfolio management strategies draw from the private venture capital playbooks. These models of innovation may work to an extent for some stakeholders at the early stages of innovation but create glaring holes for others at later stages (see sections on the "valley of death" and "scale-up" funding).
- **Regional Analysis.** Domestic semiconductor manufacturing is concentrated in several hubs around the country including Silicon Valley, Boston, and Upstate New York. Analyzing the local incentives to locate the NSTC in a given region would be valuable, both from a business environment perspective and from a state-government financing perspective.
    - In addition, it would be fruitful to investigate how other countries, namely Japan, South Korea, China, and Taiwan have fostered their semiconductor industries. Comparing and contrasting the strengths and weaknesses of these programs would be very informative for setting American policies.

About the Technology and Public Purpose (TAPP) Project

The arc of innovative progress has reached an inflection point. It is our responsibility to ensure it bends toward public good.

Technological change has brought immeasurable benefits to billions through improved health, productivity, and convenience. Yet as recent events have shown, unless we actively manage their risks to society, new technologies may also bring unforeseen destructive consequences.

Making technological change positive for all is the critical challenge of our time. We ourselves - not only the logic of discovery and market forces - must manage it. To create a future where technology serves humanity as a whole and where public purpose drives innovation, we need a new approach.

Found by former U.S. Secretary of Defense Ash Carter, the TAPP Project works to ensure that emerging technologies are developed and managed in ways that serve the overall public good.

TAPP Project Principles:

1. Technology's advance is inevitable, and it often brings with it much progress for some. Yet, progress for all is not guaranteed. We have an obligation to foresee the dilemmas presented by emerging technology and to generate solutions to them.

2. There is no silver bullet; effective solutions to technology-induced public dilemmas require a mix of government regulation and tech-sector self-governance. The right mix can only result from strong and trusted linkages between the tech sector and government.

3. Ensuring a future where public purpose drives innovation requires the next generation of tech leaders to act; we must train and inspire them to implement sustainable solutions and carry the torch.

For more information, visit: www.belfercenter.org/TAPP

Endnotes

1 CHIPS Research and Development Office, A Vision and Strategy for the National Semiconductor Technology Center (Washington, DC: National Institute of Standards and Technology (NIST), 2023), https://www.nist.gov/system/files/documents/2023/04/27/A%20Vision%20and%20Strategy%20for%20the%20NSTC.pdf.

2 Gluck, Justine, Kanwalinder Sodhi, Ariel Higuchi and Amritha Jayanti. "Community Colleges and the Semiconductor Workforce." Belfer Center for Science and International Affairs, Harvard Kennedy School, June 2023.

3 CHIPS Research and Development Office, The National Semiconductor Technology Center: Update to the Community (Washington, DC: NIST, 2022), https://www.nist.gov/system/files/documents/2022/11/18/CHIPS%20NSTC%20Update%20to%20the%20Community.pdf.

4 CHIPS Research and Development Office, A Vision and Strategy for the National Semiconductor Technology Center.

5 Ibid.

6 Ibid.

7 Ibid.

8 Graham Grose, "Demand for Digital Is on the Rise and Military Organizations Are Responding in Quick Time," Military Embedded Systems, September 13, 2021, https://militaryembedded.com/comms/communications/demand-for-digital-is-on-the-rise-and-military-organizations-are-responding-in-quick-time; Kelley M. Sayler, Artificial Intelligence and National Security, Congressional Research Service, R45178 (Washington, DC: Congressional Research Service, 2020), https://sgp.fas.org/crs/natsec/R45178.pdf; Semiconductor Industry Association, "2022 Factbook" (PowerPoint presentation, May 2022), https://www.semiconductors.org/wp-content/uploads/2022/05/SIA-2022-Factbook_May-2022.pdf.

9 Chris Miller, Chip War: The Fight for the World's Most Critical Technology (New York: Simon and Schuster, 2022).

10 VLSI Research and Semiconductor Industry Association, 2020: State of the U.S. Semiconductor Industry (Washington, DC: Semiconductor Industry Association, 2020), https://www.semiconductors.org/wp-content/uploads/2020/07/2020-SIA-State-of-the-Industry-Report-FINAL-1.pdf.

11 Miller, Chip War.

12 U.S. Government Accountability Office (GAO), Offshoring: U.S. Semiconductor and Software Industries Increasingly Produce in China and India, Report to Congressional Committees, GAO-06-423 (Washington, DC: GAO, 2006), https://www.gao.gov/assets/gao-06-423.pdf.

13 Xinhua, "China's Top Legislature Wraps Up Annual Session," NPC & CPPCC Annual Sessions 2021, March 11, 2021, http://www.xinhuanet.com/english/2021-03/11/c_139803641.htm.

14 GAO, China's New Semiconductor Policies: Issues for Congress, Congressional Research Service, CRS R46767 (Washington, DC: GAO, 2021), https://crsreports.congress.gov/product/pdf/R/R46767.

15 Willy C. Shih, "Global Supply Chains in a Post-Pandemic World," Harvard Business Review (September–October 2020), https://hbr.org/2020/09/global-supply-chains-in-a-post-pandemic-world.

16 Cagan Koc, "ASML's Factory Fire May Have Hit Output of Key Chip Machines," Bloomberg, January 7, 2022, https://www.bloomberg.com/news/articles/2022-01-07/asml-s-factory-fire-damaged-production-of-key-chip-machines#xj4y7vzkg.

17 Agathe Demarais, "How the U.S.-Chinese Technology War Is Changing the World," Foreign Policy, November 19, 2022, https://foreignpolicy.com/2022/11/19/demarais-backfire-sanctions-us-china-technology-war-semiconductors-export-controls-biden/.

18 Bradley Martin et al., Supply Chain Interdependence and Geopolitical Vulnerability: The Case of Taiwan and High-End Semiconductors (Santa Monica, CA: RAND Corporation, 2023), https://www.rand.org/pubs/research_reports/RRA2354-1.html. Also available in print form.

19 Sujai Shivakumar, Charles Wessner, and Thomas Howell, "The Strategic Importance of Legacy Chips," Center for Strategic and International Studies, March 3, 2023, https://www.csis.org/analysis/strategic-importance-legacy-chips.

20 Sarah Ravi, "2023 Factbook," Semiconductor Industry Association, May 5, 2023, https://www.semiconductors.org/resources/factbook/.

21 Ondrej Burkacky, Marc de Jong, and Julia Dragon, "Strategies to Deal with the Semiconductor Shortage," McKinsey & Company, April 15, 2022, https://www.mckinsey.com/industries/semiconductors/our-insights/strategies-to-lead-in-the-semiconductor-world; James G. March, "Exploration and Exploitation in Organizational Learning," Organization Science 2, no. 1 (1991): 71–87., http://www.jstor.org/stable/2634940.

22 "Cramming More Components onto Integrated Circuits: Moore's Law," Intel, accessed May 8, 2023, https://www.intel.com/content/www/us/en/history/virtual-vault/articles/moores-law.html.

23 Charles Weiss and William B. Bonvillian, "Complex, Established 'Legacy' Sectors: The Technology Revolutions That Do Not Happen," Innovations: Technology, Governance, Globalization 6, no. 2 (2011): 157–87, https://doi.org/10.1162/inov_a_00075.

24 Gina M. Raimondo, "Remarks by U.S. Secretary of Commerce Gina Raimondo: The CHIPS Act and a Long-Term Vision for America's Technological Leadership," Office of Public Affairs, U.S. Department of Commerce, February 23, 2023, https://www.commerce.gov/news/speeches/2023/02/remarks-us-secretary-commerce-gina-raimondo-chips-act-and-long-term-vision.

25 Gordon E. Moore, "Cramming More Components onto Integrated Circuits," Electronics 38, no. 8 (1965): 114–117.

26 Burkacky, De Jong, and Dragon, "Strategies to Deal with the Semiconductor Shortage."

27 CHIPS Research and Development Office, A Vision and Strategy for the National.

28 National Institute of Standards and Technology, "Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry" (Washington, DC: U.S. Department of Commerce, 2022), https://doi.org/10.6028/nist.sp.1282.

29 "Living Its Legacy: IMEC—Independent R&D Hub for Nano- and Digital Technologies," imec, accessed May 9, 2023, https://www.imec-int.com/en/about-imec/history.

30 "IMEC Offers Neutral Ground amid Chip Rivalries," Economist, September 22, 2021, https://www.economist.com/business/imec-offers-neutral-ground-amid-chip-rivalries/21804980.

31 "Microelectronics Laboratory," MIT Lincoln Laboratory, accessed May 9, 2023, https://www.ll.mit.edu/about/facilities/microelectronics-laboratory.

32 Frank Tietze, "Empowering SMEs to Leverage IP for Innovation," WIPO, June 2021, https://www.wipo.int/wipo_magazine/en/2021/02/article_0003.html.

33 CHIPS Research and Development Office, A Vision and Strategy for the National.

34 "The Success of Bayh-Dole," (factsheet, PhRMA, accessed May 9, 2023), https://www.phrma.org/-/media/Project/PhRMA/PhRMA-Org/PhRMA-Org/PDF/S-U/The-Success-of-Bayh-Dole_Pocket-Card_FINAL.PDF.

35 Brian Dunbar, "Commercial Orbital Transportation Services (COTS)," Commercial Space Economy, NASA, August 3, 2017, https://www.nasa.gov/commercial-orbital-transportation-services-cots; Karen L. Howard and Candice N. Wright, "Operation Warp Speed: Accelerated COVID-19 Vaccine Development Status and Efforts to Address Manufacturing Challenges," U.S. Government Accountability Office, February 11, 2021, https://www.gao.gov/products/gao-21-319.

36 David Adler, "Inside Operation Warp Speed: A New Model for Industrial Policy," American Affairs 5, no. 2 (Summer 2021): 3–32, https://americanaffairsjournal.org/2021/05/inside-operation-warp-speed-a-new-model-for-industrial-policy/.

37 Melissa C. Lott, "Solyndra: Illuminating Energy Funding Flaws?," Scientific American, September 27, 2011, https://blogs.scientificamerican.com/plugged-in/solyndra-illuminating-energy-funding-flaws/.

38 William B. Bonvillian, "Industrial Innovation Policy in the United States," Annals of Science and Technology Policy 6 (4): 315–411, https://doi.org/10.1561/110.00000026; Adler, "Inside Operation Warp Speed."

39 Alan Ho and Jake Taylor, "Using Advance Market Commitments for Public Purpose Technology Development," Belfer Center for Science and International Affairs, Policy Brief, June 2021, https://www.belfercenter.org/publication/using-advance-market-commitments-public-purpose-technology-development.

40 "Defense Production Act Title III Presidential Determination for Printed Circuit Boards and Advanced Packaging Production Capability," press release, U.S. Department of Defense, March 27, 2023, https://www.defense.gov/News/Releases/Release/Article/3342032/defense-production-act-title-iii-presidential-determination-for-printed-circuit/.

41 "U.S. Department of Commerce Announces Chips for America R&D Leaders," press release, NIST, June 6, 2023, https://www.nist.gov/news-events/news/2023/06/us-department-commerce-announces-chips-america-rd-leaders.